

Fig. 1

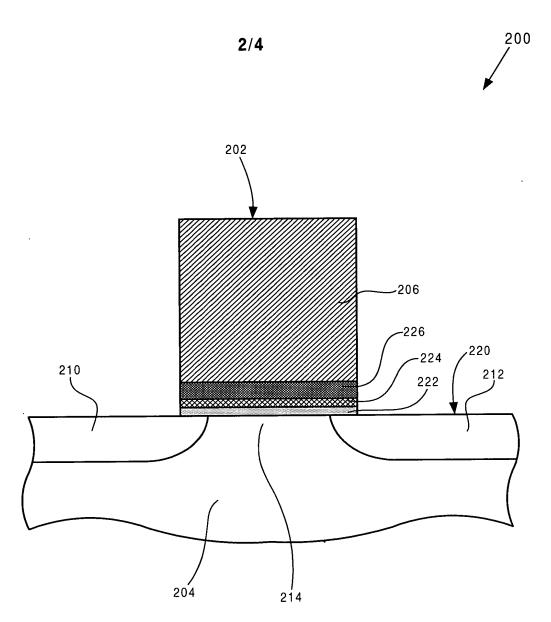


Fig. 2



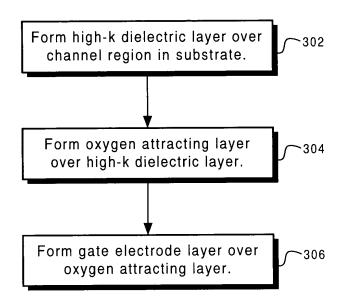


Fig. 3

400

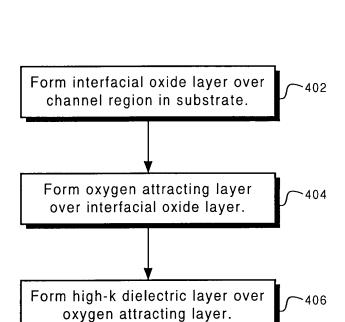


Fig. 4

Form gate electrode layer over high-k dielectric layer.